AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Richard E. Fackenthal	§	Art Unit:	2133
Serial No.:	10/687,124	§	Examiner:	Guy J. Lamarre
Filed:	October 16, 2003	§	Atty Docket:	ITL.1046US (P17448)
For:	Error Correction for Multi-Level Cell Memory with Overwrite Capability	§	Assignee:	Intel Corporation

Mail Stop **Appeal Brief**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF AMENDED APPEAL BRIEF

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief, attached hereto is an Amended Appeal Brief.

In the Summary of Claimed Subject Matter section, the reference figures for claim 38 have been corrected. The Amended Appeal Brief is therefore believed to be in compliance.

No fee is believed to be due with this response. However, the Commissioner is authorized to charge any fee due to Deposit Account No. 20-1504 (ITL.1046US).

Respectfully submitted,

Date: July 17, 2007

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Date of Deposit: July 17, 2007
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.
Nancy Meshkoff

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Nancy Meshkoff

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-48 (Rejected).

Claims 1-48 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method comprising:

selectively storing data in a memory array at different densities per cell (Figure 5, 230) (specification at page 8, line 16 to page 9, line 11); and

implementing error correction depending on the density of data storage (Figure 5, 240) (specification at page 7, line 25 to page 8, line 6).

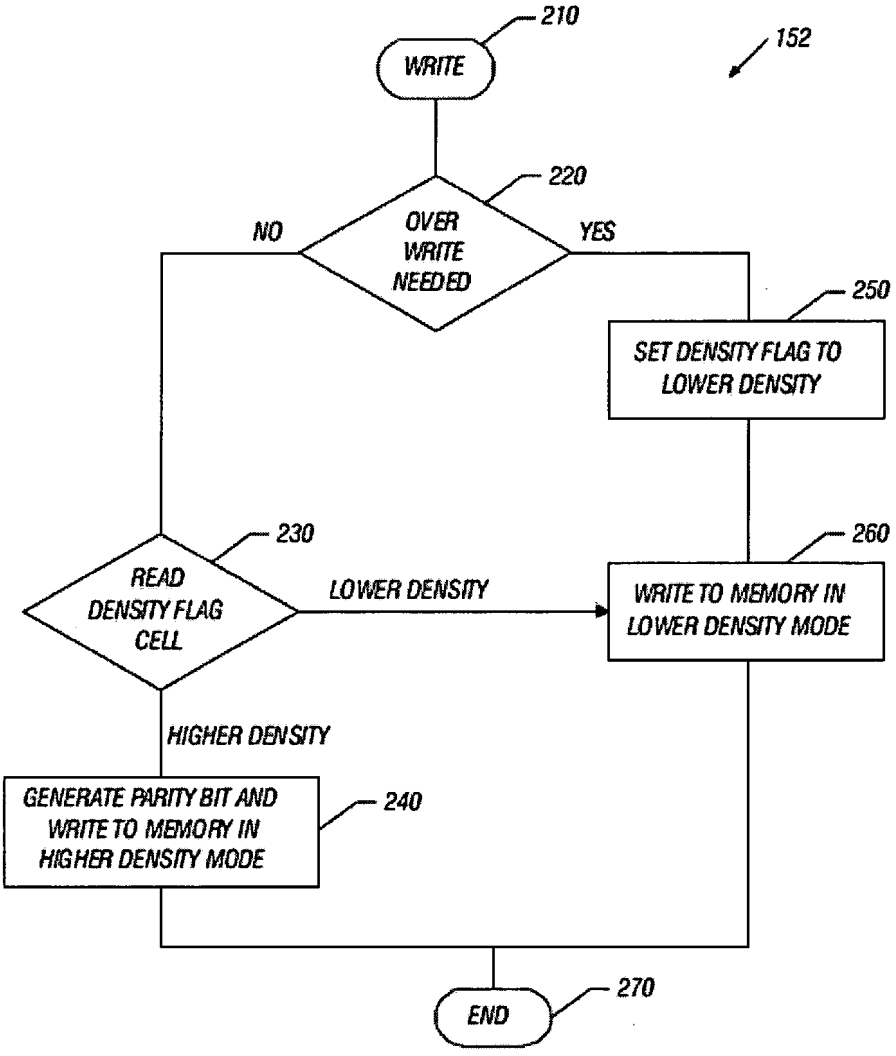

FIG. 5

15. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

selectively store data in a memory array at different densities per cell (Figure 5, 230) (specification at page 8, line 16 to page 9, line 11); and

implement error correction depending on the density of data storage (Figure 5, 240) (specification at page 7, line 25 to page 8, line 6).

29. A memory comprising:

a memory array (Figure 1, 160); and

a controller (Figure 1, 150) coupled to said memory array to selectively store data in the memory array at different densities per cell (Figure 5, 230) (specification at page 8, line 16 to page 9, line 11) and to implement error correction depending on the density of data storage (Figure 5, 240) (specification at page 7, line 25 to page 8, line 6).

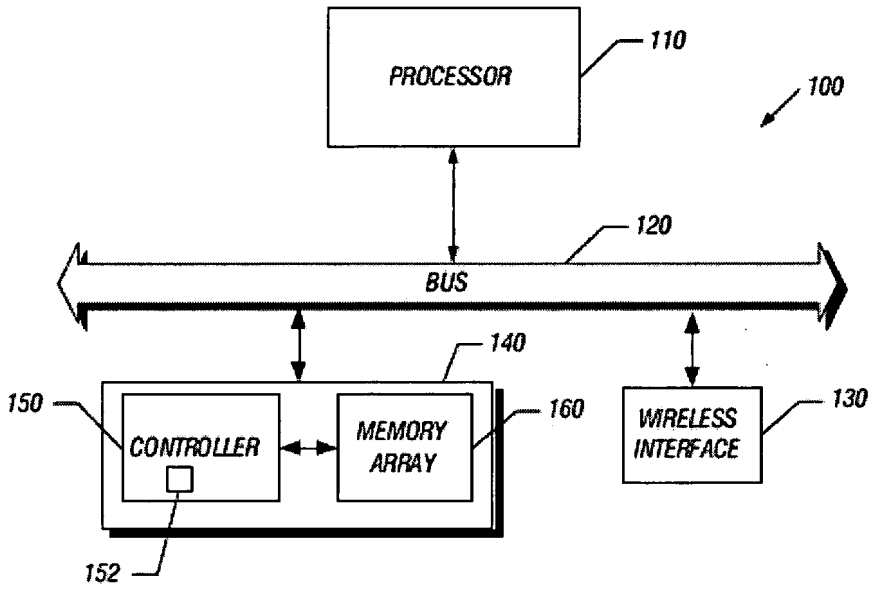

FIG. 1

38. A system comprising:

a processor (Figure 1, 110);

a wireless interface (Figure 1, 130);

a memory (Figure 1, 160) coupled to said processor; and

a controller (Figure 1, 150) coupled to said memory to selectively store data in said memory at different densities per cell (Figure 5, 230) (specification at page 8, line 16 to page 9, line 11) and to implement error correction depending on a density of data storage (Figure 5, 240) (specification at page 7, line 25 to page 8, line 6).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-48 are anticipated under 35 U.S.C. § 102(b) by Gregoti ("Construction of Polyvalent Error Control Codes for Multilevel Memories," pp. 751-754, IEEE, 2000).

ARGUMENT

A. Are claims 1-48 anticipated under 35 U.S.C. § 102(b) by Gregoti ("Construction of Polyvalent Error Control Codes for Multilevel Memories," pp. 751-754, IEEE, 2000)?

Claim 1 calls for storing data in a memory array at different densities per cell. Further, it calls for implementing error correction depending on the density of data storage.

The cited reference to Gregori talks about a multi-level memory (ML). He also talks, in the paragraph above Section III on page 752, about the case where ML memories work at variable number of bits per cell. He there explains that the requested error correction capability must be determined for the operating mode with the worst cell error probability (i.e. the operating mode with the highest number of bits per cell). Thus, Gregori is explicit that he does not change the error correction capability depending on the number of bits per cell. Instead, he determines the worst case and sets that as the default regardless of the number of bits per cell. Therefore, clearly, Gregori cannot teach the claimed invention.

This is further confirmed in Figure 3 and the material cited on page 754. The input transcoder receives the input c. It also receives a 4-ary/16-ary source word and converts it to a 16-ary source word. The error correction though is not carried out until later, as indicated in the next paragraph. On the basis of the 36 16-ary digit word, the decoder, all the way in the right column of Figure 3, actually does the error coding. All the block with the c input does is convert everything to a 16-ary source word. Thus, the source word is the same regardless of the number of bits per cell. This has no effect on error correction and is simply conforming to a standard value prior to error correction. This is completely consistent with the language previously discussed on page 752. As described earlier, the error correction code simply takes the worst case and applies that across the board.

The advisory action misreads the cited material at page 752 which calls for "a" (i.e. one), polyvalent code for a memory operating at two and four bits per cell. This suggests a "one size fits all" approach to error correction.

Therefore, the rejection of claim 1 should be reversed.

On the same basis, the rejections of claims 15, 29, and 38 should be reversed.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: July 17, 2007

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CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:
selectively storing data in a memory array at different densities per cell; and
implementing error correction depending on the density of data storage.

2. The method of claim 1 including selectively storing data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.

3. The method of claim 2 including using a higher density mode with double the number of threshold levels as a lower density mode.

4. The method of claim 3 including using a higher density mode with four threshold levels and a lower density mode using two threshold levels.

5. The method of claim 1 wherein implementing error correction code depending on the density of data storage includes determining whether data is in a higher or lower density mode and if the data is in a higher density mode, implementing error correction code and if the data is in a lower density mode, omitting error correction code.

6. The method of claim 5 including using a flag to indicate whether or not the data is in a lower or higher density mode.

7. The method of claim 5 including allowing overwriting when the data is stored in the lower density mode.

8. The method of claim 7 including preventing overwriting when the data is stored in the higher density mode.

9. The method of claim 1 including allowing overwriting of stored data when error correcting codes are not provided for that data.

10. The method of claim 1 including providing a multi-level memory cell array having a capacity of at least four levels.

11. The method of claim 10 including using at least two bits to represent said at least four levels.

12. The method of claim 11 including using one of said bits as a more significant bit and the other of said bits as a less significant bit.

13. The method of claim 12 wherein data from at least two cells forms a codeword and grouping the more significant bits from different cells together.

14. The method of claim 13 including providing more significant bits in one half of a word and less significant bits in the other half of a word.

15. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

selectively store data in a memory array at different densities per cell; and

implement error correction depending on the density of data storage.

16. The article of claim 15 further storing instructions that, if executed, enable the system to selectively store data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.

17. The article of claim 16 further storing instructions that, if executed, enable the system to use a higher density mode with double the number of threshold levels as a lower density mode.

18. The article of claim 17 further storing instructions that, if executed, enable the system to use a higher density mode with four threshold levels and a lower density mode using two threshold levels.

19. The article of claim 15 further storing instructions that, if executed, enable the system to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implement error correction code and if the data is in a lower density mode, omit error correction code.

20. The article of claim 19 further storing instructions that, if executed, enable the system to use a flag to indicate whether or not the data is in a lower or higher density mode.

21. The article of claim 19 further storing instructions that, if executed, enable the system to allow overwriting when the data is stored in a higher density mode.

22. The article of claim 20 further storing instructions that, if executed, enable the system to prevent overwriting when data is stored in the higher density mode.

23. The article of claim 15 further storing instructions that, if executed, enable the system to allow overwriting of stored data when error correcting codes are not provided for that data.

24. The article of claim 15 further storing instructions that, if executed, enable the system to provide a multi-level memory cell array having a capacity of at least four levels.

25. The article of claim 24 further storing instructions that, if executed, enable the system to use at least two bits to represent said at least four levels.

26. The article of claim 25 further storing instructions that, if executed, enable the system to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

27. The article of claim 26 wherein data from at least two cells forms a codeword and further storing instructions that, if executed, enable the system to group the more significant bits from different cells together.

28. The article of claim 27 further storing instructions that, if executed, enable the system to provide more significant bits in one half of a codeword and less significant bits in the other half of a codeword.

29. A memory comprising:

a memory array; and

a controller coupled to said memory array to selectively store data in the memory array at different densities per cell and to implement error correction depending on the density of data storage.

30. The memory of claim 29 wherein said memory array is a multi-level flash memory array.

31. The memory of claim 29 wherein said controller to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implement error correction and if the data is in a lower density mode, omit error correction.

32. The memory of claim 31 said controller to allow overwriting when the data is stored in the lower density mode.

33. The memory of claim 32 said controller to prevent overwriting when the data is stored in the higher density mode.

34. The memory of claim 29 said controller to allow overwriting of stored data when error correcting code is not provided for that data.

35. The memory of claim 29 said controller to use at least two bits to represent four threshold voltage levels.

36. The memory of claim 35 said controller to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

37. The memory of claim 36 said controller to group the more significant bits from different cells together.

38. A system comprising:

a processor;

a wireless interface;

a memory coupled to said processor; and

a controller coupled to said memory to selectively store data in said memory at different densities per cell and to implement error correction depending on a density of data storage.

39. The system of claim 38 wherein said memory is a multi-level flash memory.

40. The system of claim 38 wherein said controller to determine whether data is in higher or lower density mode and if the data is in a higher density mode, implement error correction and if the data is in a lower density mode, omit error correction.

41. The system of claim 40 said controller to allow overwriting when the data is stored in the lower density mode.

42. The system of claim 41 said controller to prevent overwriting when the data is stored in the higher density mode.

43. The system of claim 38 said controller to allow overwriting of stored when error correcting codes are not provided for that data.

44. The system of claim 38 said controller to use at least two bits to represent four threshold levels.

45. The system of claim 44 said controller to use one of said bits as a more significant bit and the other said bits as a less significant bit.

46. The system of claim 45 said controller to group the more significant bits from different cells together.

47. The system of claim 38 wherein said wireless interface includes an antenna.

48. The system of claim 47 wherein said wireless interface includes a dipole antenna.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.